REMARKS

In this Amendment, Applicant adds new claims 37-40. Accordingly, claims 1-26 and 29-40 are all the claims pending in the application. The new claims are at least supported by paragraph [0043] of the instant specification. Claims 8-15 and 22-26 are withdrawn from consideration.

Claim rejection under 35 U.S.C. § 103(a)

Claims 1, 3-4, 17-19, 21, 29-35 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yanagi et al. (U. S. Patent No. 7,002,541 B2; hereinafter "Yanagi") in view of Okajima (U.S. Patent No. 5,793,680; hereinafter "Okajima") and Yatabe et al. (Japanese Publication No. 2001-051662 as translated by U.S. Patent No. 6,633,287 B1; hereinafter "Yatabe").

Claims 5, 20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yanagi in view of Okajima, Yatabe and Park et al. (U.S. Patent No. 7,133,034; hereinafter "Park").

Claims 2, 6-7, 16, 36 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yanagi in view of Okajima, Yatabe, Kubota et al. (U.S. Publication No. 2002/0075249; hereinafter "Kubota") and Nagai (U.S. Patent No. 6,011,355; hereinafter "Nagai"). and Park.

Applicant traverses the rejection as follows.

Claim 1

Claim 1 recites, *inter alia*, "a high level of a signal passing through the at least one signal line is higher than the high level voltage signal supplied by said first voltage supply and a low level of the signal passing through the signal line is lower than the low level voltage signal supplied by said second voltage supply." The Examiner acknowledges that Yanagi does not teach these features of claim 1, but contends that Yatabe allegedly discloses these features. See page 4 of the Office Action.

Applicant respectfully disagrees for at least the following reasons.

Yatabe is directed to a power supply circuit of an electro-optical device with a fewer externally mounted components. In FIG. 5, Yatabe discloses an illustration of a polarity inverting operation in the power supply circuit. However, Yatabe does not teach or suggest "a high level of a signal passing through the at least one signal line is higher than the high level voltage signal supplied by said first voltage supply and a low level of the signal passing through the signal line is lower than the low level voltage signal supplied by said second voltage supply."

In FIG. 5, Yatabe discloses a relationship of high and low voltages put to a line that is VSN < GND < Vcc < VSP. However, Yatabe does not teach or suggest that the high voltage of a signal line is VSP and low voltage of a signal line is VSN. Therefore, Yatabe does not teach or suggest the above-mentioned features of claim 1.

In fact, the disclosure in FIG. 4 of Yatabe, clearly shows that the teaching of Yatabe is different from the above-mentioned features of claim 1. In particular, referring to FIG. 4 of Yatabe, when terminal "a" of switch SW 1 and terminal "a" of switch SW 2 are selected, electric potential of terminal "c" of SW 1 becomes high level VSP and electric potential of terminal "c" of SW 2 becomes ground level GND. Therefore, electric potential of Cp becomes VSP. The VSP corresponds to the VSP shown in FIG. 5 of Yatabe.

On the other hand, when terminal "b" of SW 1 and terminal "b" of SW2 are selected, electric potential of terminal "c" of SW 1 becomes Vcc and electric potential of terminal c of SW 2 becomes low level VSN. The low level VSN is obtained by subtracting VSP, which is the electric potential of Cp, from Vcc. The VSN corresponds to the VSN shown in FIG. 5 of Yatabe. In other words, VSN

is obtained by reversing the positive electric potential of VSP on the basis of the middle electric potential VC of Vcc. However, Yatabe does not teach or suggest a signal of which high level is VSP and low level is VSN being output from any terminals.

As such, Yatabe does not teach or suggest "a high level of a signal passing through the at least one signal line is higher than the high level voltage signal supplied by said first voltage supply and a low level of the signal passing through the signal line is lower than the low level voltage signal supplied by said second voltage supply."

Moreover, claim 1 further requires that the at least one signal line connected to each gate terminal of said first and second transistors, which controls the switching of the first and second transistors. However, Yatabe does not teach this feature of claim 1. As such, it would be improper for Yatabe to disclose that a high level of a signal passing through the at least one signal line (which is connected to each gate terminal of said first and second transistors, which controls the switching of the first and second transistors) higher than the high level voltage signal supplied by said first voltage supply and a low level of the signal passing through the signal line is lower than the low level voltage signal supplied by said second voltage supply.

Furthermore, even if, *assuming arguendo*, the teachings of Yatabe and Okajima were to be combined as proposed by the Examiner, the combination would not teach that the at least one signal line connected to each gate terminal of said first and second transistors, which controls the switching of the first and second transistors, wherein a high level of a signal passing through the at least one signal line is higher than the high level voltage signal supplied by said first voltage supply and a low

level of the signal passing through the signal line is lower than the low level voltage signal supplied by said second voltage supply.

In view of the above Applicant respectfully submits that claim 1 is patentable over the cited combination of references.

Claims 17, 33 and 34

Applicants respectfully submit that claims 17, 33 and 34 recite subject matter analogous to claim 1, and therefore are allowable for at least analogous reasons claim 1 is allowable.

Claims 3-4, 18-19, 21, 29-32 and 35

Applicants submit that claims 3-4, 18-19, 21, 29-32 and 35 depend from one of the independent claims that have been shown to be allowable, and therefore these claims are allowable at least by virtue of there dependency and the additional features recited therein.

With regard to claims 29-32, Applicant respectfully submits that the features of these claims are not disclosed in the combination of Yanagi, Okajima and Yatabe.

For instance, resistances 5a and 5b in an offset voltage setting section 5 shown in FIG. 1 of Yanagi are used for dividing the voltage of Vrefl. However, this does not teach or suggest a level shift circuit. Further, element 60 of FIG. 14 of Okajima corresponds to a CLOCK-PULSE-ARRANGEMENT DETERMINATION UNIT. However, there is no description for item 60 to have the function of conversion of the level of the input signal, and therefore does not teach or suggest a level shift circuit as recited in claims 29-32.

Claims 5 and 20

Applicant submits that since claims 5 and 20 depend from one of the claims that have been shown to be allowable and since Park does not teach or suggest the features of claim 1 missing in Yanagi, Yatabe and Okajima, these claims are also allowable at least by virtue of their dependency and the additional features recited therein.

With regard to claims 5 and 20, the Examiner cites Park for allegedly disclosing "wherein a high-level voltage of each signal of said signal line and said inversion signal line is a high-level line voltage of said gate driver and wherein a low-level voltage of each signal of said signal line and said inversion signal line is a low-level line voltage of said gate driver." Applicant respectfully disagrees with the Examiner for at least the following reasons.

Applicant respectfully submits that although Park discloses a signal controller input to the driver (FIG. 1), Park does not teach or suggest a high-level voltage of each signal of said signal line and said inversion signal line is a high-level line voltage of said gate driver and wherein a low-level voltage of each signal of said signal line and said inversion signal line is a low-level line voltage of said gate driver, as recited in claims 5 and 20.

Claims 2, 6-7, 16, 36

Applicants submit that since claims 2, 6-7, 16, 36 depend from one of the claims that have been shown to be allowable and since Kubota, Nagai and Park do not teach or suggest the features of claim 1 missing in Yanagi, Yatabe and Okajima, these claims are also allowable at least by virtue of their dependency and the additional features recited therein.

New claims

Claims 37-40 depend from one of the claims that is shown to be patentable, and therefore, these claims are patentable at least by virtue of their dependency and the additional features recited therein.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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Date: September 15, 2010